CLAIMS

What is claimed is:

1. An adaptive analog-to-digital converter (ADC) system comprising:

an automatic gain control (AGC) controller for receiving both in-band and out-of-band signals from a radio frequency (RF) receiver and producing an AGC control signal therefrom;

a digital signal processor (DSP) for interpreting the AGC control signal and providing at least one adjustment signal to an ADC; and

wherein the ADC uses the at least one adjustment signal to control current drain based upon an RF signal received by the AGC controller.

2. An adaptive ADC system as in claim 1, wherein the AGC controller receives an on-channel signal and an in-band detection signal for determining the amount of off-channel interference received by the RF receiver.

3. An adaptive ADC system as in claim 2, wherein the AGC controller processes an input to the ADC, an output from the ADC and an RF signal input for producing at least one radio signal strength indication (RSSI) signal used as the ADC control signal.

4. An adaptive ADC system as in claim 1, wherein the at least one adjustment signal adjusts quantizer bit resolution.

5. An adaptive ADC system as in claim 1, wherein the at least one adjustment signal controls current bias used by a bit quantizer in the ADC.

6. An adaptive ADC system as in claim 1, wherein the at least one adjustment signal adjusts the size of a reference capacitance in the ADC.

7. An adaptive ADC system as in claim 1, wherein the at least one adjustment signal adjusts the current bias used by a reference capacitance in the ADC.

8. An adaptive ADC system as in claim 1, wherein the at least one adjustment signal adjusts over-sampled clock speed in the ADC.

9. An adaptive analog-to-digital converter (ADC) system that utilizes digital signal processing to control operational parameters of an ADC comprising:

an automatic gain control (AGC) controller for receiving at least one input signal from a radio frequency (RF) receiver and providing an AGC control signal in response thereto;

a digital signal processor (DSP) for receiving the AGC control signal and providing at least one adaptive ADC control signal based on desired communication protocol requirements; and

an ADC for converting received analog input signals to a digital format and dynamically controlling current drain based upon the at least one adaptive control signal.

10. An adaptive ADC system as in claim 9, wherein the AGC controller receives both a sum-of-squares (SOS) signal from an RF receiver and an in-band signal for determining the quality of a received RF input signal.

11. An adaptive ADC system as in claim 9, wherein the AGC controller receives an input to the ADC, an output from the ADC and the at least one input signal.

12. An adaptive ADC system as in claim 11, wherein the AGC controller produces a received signal strength indication (RSSI) control signal based upon the SOS signal and the in-band signal.

13. An adaptive ADC system as in claim 12, wherein the RSSI signal is provided to the DSP for dynamically controlling the at least one adaptive control signal.

14. An adaptive ADC system as in claim 9, wherein the at least one adaptive ADC control signal controls the number of bits used by an ADC quantizer.

15. An adaptive ADC system as in claim 9, wherein the at least one adaptive ADC control signal controls the amount of current used by an ADC quantizer.

16. An adaptive ADC system as in claim 9, wherein the at least one adaptive ADC control signal controls the amount of reference capacitance used by the ADC.

17. An adaptive ADC system as in claim 9, wherein the at least one adaptive ADC control signal controls the amount of charging current used by a reference capacitance in the ADC.

18. An adaptive ADC system as in claim 9, wherein the at least one adaptive ADC control signal controls clock speed of the ADC.

19. A method for adjusting the operational parameters of an analog-to-digital converter (ADC) for providing optimal performance with minimum current drain comprising the steps of:

receiving a radio frequency (RF) input signal from a receiver;

producing at least one automatic gain control (AGC) control signal from the received RF input signal;

processing the AGC control signal using a digital signal processor to provide at least one adjustment control signal; and

receiving the at least one adjustment control signal at an ADC where the at least one adjustment control signal is used to control functionality of the ADC to maximize efficiency based upon the received RF input signal.

20. A method for adjusting the operational parameters of an ADC as in claim 19, further comprising the step of:

utilizing a sum-of-squares signal calculation and an in-band signal to produce the at least one AGC control signal.

21. A method for adjusting the operational parameters of an ADC as in claim 20, wherein the at least one AGC control signal is a radio signal strength indication (RSSI) signal.

22. A method for adjusting the operational parameters of an ADC as in claim 19, wherein the AGC control signal is processed based on desired communications protocol requirements.

23. A method for adjusting the operational parameters of an ADC as in claim 19, wherein the at least one adjustment control signal controls quantizer bit resolution in the ADC.

24. A method for adjusting the operational parameters of an ADC as in claim 19, wherein the at least one adjustment control signal controls bias current used by a quantizer in the ADC.

25. A method for adjusting the operational parameters of an ADC as in claim 19, wherein the at least one adjustment control signal controls the amount of reference capacitance used in the ADC.

26. A method for adjusting the operational parameters of an ADC as in claim 19, wherein the at least one adjustment control signal controls the amount of charging bias used by a reference capacitance in the ADC.

27. A method for adjusting the operational parameters of an ADC as in claim 19, wherein the at least one adjustment control signal controls the reference clock speed of the ADC.